- Multiplexed Inputs/Outputs Provide Improved Bit Density
- Four Modes of Operations:

Hold (Store)
Shift Right

Shift Left Load Data

- Operates with Outputs Enabled or at High Z
- 3-State Outputs Drive Bus Lines Directly
- Can Be Cascaded for N-Bit Word Lengths
- SN54LS323 and SN74LS323 Are Similar But Have Synchronous Clear
- Applications:

Stacked or Push-Down Registers Buffer Storage, and Accumulator Registers

	GUARANTEED	TYPICAL
TYPE	SHIFT (CLOCK)	POWER
	FREQUENCY	DISSIPATION
'LS299	25 MHz	175 mW
'S299	50 MHz	700 mW

SN54LS299, SN54S299 . . . J OR W PACKAGE SN74LS299, SN74S299 . . . DW OR N PACKAGE (TOP VIEW)

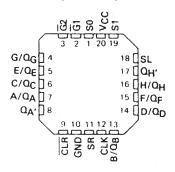
SO 1 2 19 51

G2 3 18 5L

G/QG 4 17 0H'

F/OE 5 16 H/OH

SN54LS299, SN54S299 . . . FK PACKAGE (TOP VIEW)



#### description

These Schottky TTL eight-bit universal registers feature multiplexed inputs/outputs to achieve full eight-bit data handling in a single 20-pin package. Two function-select inputs and two output-control inputs can be used to choose the modes of operation listed in the function table.

Synchronous parallel loading is accomplished by taking both function-select lines, S0 and S1, high. This places the three-state outputs in a high-impedance state, which permits data that is applied on the input/output lines to be clocked into the register. Reading out of the register can be accomplished while the outputs are enabled in any mode. A direct overriding input is provided to clear the register whether the outputs are enabled or off.

#### **FUNCTION TABLE**

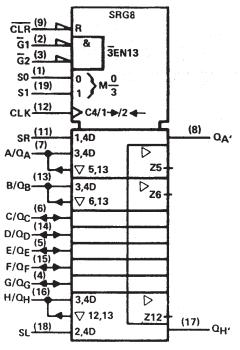
				INPL	ITS						IN	PUTS/0	OUTPU	TS			OUT	PUTS
MODE	CLR	FUNC	ECT		TPUT TROL	CLK	SEF	RIAL	A/Q <sub>A</sub>	B/QB	c/Q <sub>C</sub>	D/QD	E/QE	F/Q <sub>F</sub>	G/Q <sub>G</sub>	H/QH	Q <sub>A</sub> ,	Q <sub>H</sub>
		S1	<b>S0</b>	Ğ1 <sup>†</sup>	Ğ2 <sup>†</sup>		SL	SR					_					
	L	х	L	L	L	×	Х	Х	L	L	L	L	L	L	L	L	L	, L
Clear	L	L.	Х	L	L	×	X	X	L	L	L	L	L	L	L	L.	L	L
	L	Н	н	Х	Х	×	X	X	×	X	X	×	X	Х	×	×	L	L
Hold	Н	L	L	L	^L	×	×	×	QAO	Ово	aco	Q <sub>D0</sub>	QEO	Q <sub>F0</sub>	Q <sub>G0</sub>	αнο	QAO	QHO
noio	н	×	×	L	L	l L	×	×	QAO	Q <sub>BO</sub>	$a_{co}$			Q <sub>F0</sub>			1	
Shift Right	н	L	Н	L	L	t	Х	Н	Н	QAn	QBn	Q <sub>Cn</sub>	QDn	QEn	QFn	$Q_{Gn}$	Н	$a_{Gn}$
Shirt right	н	L	н	L	L		×	L	L	$Q_{An}$	$Q_{Bn}$	$a_{Cn}$	$a_{Dn}$	$\alpha_{En}$	$Q_{Fn}$	$Q_{Gn}$	L	$Q_{Gn}$
Shift Left	Н	Н	L	L	L	1	Н	×	QBn	QCn	QDn	QEn	QFn	QGn	QHn	Н	QBn	Н
Simil Left	н	Н	L	L	L	t	L	×	QBn	$\alpha_{Cn}$	$a_{Dn}$	$\alpha_{En}$	$Q_{Fn}$	$\alpha_{Gn}$	$Q_{Hn}$	L	QBn	L
Load	Н	Н	Н	Х	×	1	Х	Х	а	b	С	d	e	f	g	h	а	h

TWhen one or both output controls are high the eight input/output terminals are disabled to the high-impedance state; however, sequential operation or clearing of the register is not affected.

a...h = the level of the steady-state input at inputs A through H, respectively. These data are loaded into the flip-flops while the flip-flop outputs are isolated from the input/output terminals.

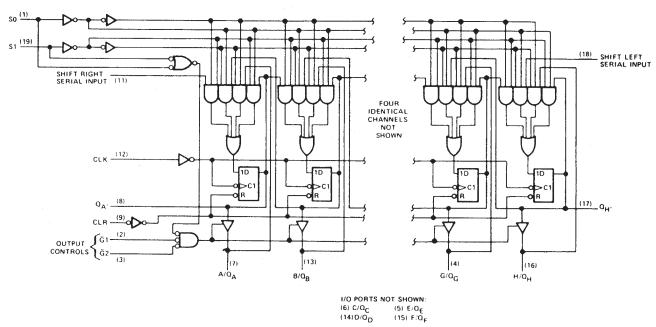


### logic symbol†



 $<sup>^\</sup>dagger$  This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for DW, J, N, and W packages.

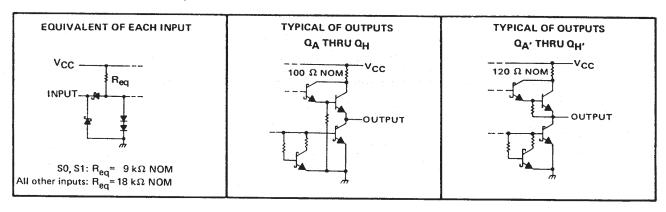
### logic diagram (positive logic)



Pin numbers shown are for DW, J, N, and W packages.



### schematics of inputs and outputs



# absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

S	upply voltage, VCC (see Note 1)																					7 V	,
- 1	nput voltage						٠.								٠.							7 V	1
C	ff-state output voltage																				5.	.5 V	,
(	perating free-air temperature range:	: S	N5	4L	.S2	99												-5	5°(	C to	12	25°C	)
_		S	N7	'4L	.S2	99													0	°C 1	o 7	o°C	;
S	torage temperature					٠												-6	5°(	Cto	15	o°C	;

NOTE 1: Voltage values are with respect to network ground terminal.

#### recommended operating conditions

		SN54LS299			SN74LS299			l <u> </u>
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Supply voltage, VCC		4.5	5	5.5	4.75	5	5.25	V
High-level output current, IOH	QA thru QH			-1			-2.6	
The state of the s	Q <sub>A</sub> ' or Q <sub>H</sub> '			0.4			-0.4	mA
Low-level output current, IOL	QA thru QH			12			24	
	Q <sub>A</sub> ' or Q <sub>H</sub> '			4			8	mA
Clock frequency, fclock		0		20	0		20	MHz
Width of clock pulse, tw(clock)	Clock high	30			30			
	Clock low	1.8			10			ns
Width of clear pulse, tw(clear)	Clear low	25			20			ns
	Select	351			351			
Setup time, t <sub>SU</sub>	High-level data <sup>†</sup>	201			201			
, <i>'</i> 50	Low-level data <sup>†</sup>	20↑			201			ns
	Clear inactive-state	241			201			
Hold time, th	Select	10↑			101			
	Data <sup>†</sup>	3†			01			ns
Operating free-air temperature, TA		-55		125	0		70	°C

<sup>&</sup>lt;sup>†</sup> Data includes the two serial inputs and the eight input/output data lines.



## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CON	NITIONS!	S	N54LS2	99	S	UNIT			
	TANAMETEN		TEST CONE	or rions .	MIN	TYP‡	MAX	MIN	TYP <sup>‡</sup>	MAX	UNIT
$v_{IH}$	High-level input voltage			-	2			2			V
VIL	Low-level input voltage						0.7			8.0	V
VIK	Input clamp voltage		V <sub>CC</sub> = MIN,	I <sub>I</sub> = -18 mA			-1.5			-1.5	V
Voн	High-level output voltage	Q <sub>A</sub> thru Q <sub>H</sub>	V <sub>CC</sub> = MIN,	V <sub>IH</sub> = 2 V,	2.4	3.2		2.4	3.1		V
VOH	riigii-ievei output voitage	QA' or QH'	VIL = VILmax,	IOH = MAX	2.5	3.4		2.7	3.4		1 °
		Q <sub>A</sub> thru Q <sub>H</sub>	V <sub>CC</sub> = MIN,	I <sub>OL</sub> = 12 mA		0.25	0.4		0.25	0.4	
VOL	Low-level output voltage	ag ma ah	V <sub>IH</sub> = 2 V,	I <sub>OL</sub> = 24 mA					0.35	0.5	V
VOL	Low-lever output vortage	QA' or QH'	VIH - 2 V, VIL = VILmax	IOL = 4 mA		0.25	0.4		0.25	0.4	1 °
		ay or all	AIF - AIFINGY	IOL = 8 mA					0.35	0.5	1
lozh	Off-state output current,	QA thru QH	V <sub>CC</sub> = MAX,	V <sub>IH</sub> = 2 V,			40			40	
'UZH	high-level voltage applied	ay ma ah	V <sub>O</sub> ≈ 2.7 V				40			40	μΑ
<sup>1</sup> OZL	Off-state output current,	Q <sub>A</sub> thru Q <sub>H</sub>	V <sub>CC</sub> = MAX,	V <sub>IH</sub> = 2 V,			-400			-400	μА
.02L	low-level voltage applied	ад ини ан	V <sub>O</sub> = 0.4 V				400			-400	μ~
	Input current at maximum	S0, S1		V1 = 7 V			200			200	
11	input voltage	A thru H	V <sub>CC</sub> = MAX	V <sub>1</sub> = 5.5 V			100			100	μА
	mput vortage	Any other		V <sub>1</sub> = 7 V			100			100	1
1	High-level input current	A thru H, SO, S1	V				40			40	
IН	rngn-iever input current	Any other	V <sub>CC</sub> = MAX,	$V_1 = 2.7 \text{ V}$			20			20	μΑ
1	Low lovel input aussent	S0, S1	V	V = 0.4 V			-0.8		······································	-0.8	
ΙΙL	Low-level input current	Any other	V <sub>CC</sub> = MAX,	$V_1 = 0.4 V$			-0.4	1		-0.4	mA
	Short sizzuit	QA thru QH	V		30		130	-30		-130	T .
IOS	Short-circuit output current 9	QA' or QH'	V <sub>CC</sub> = MAX		-20		-100	-20		-100	mA
Icc	Supply current		V <sub>CC</sub> = MAX			33	53		33	53	mA

<sup>&</sup>lt;sup>†</sup>For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

## switching characteristics, $V_{CC} = 5 \text{ V}$ , $T_A = 25^{\circ} \text{ C}$

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f <sub>max</sub>			See Note 2	20	35		MHz
<sup>t</sup> PLH	CLK	Out or Out	$R_1 = 2 k\Omega$ , $C_1 = 15 pF$		22	33	
<sup>t</sup> PHL	CLK	Q <sub>A</sub> ' or Q <sub>H</sub> '	N[ - 2 k32, C[ - 15 pr		26	39	ns
tPHL	CLR	QA' or QH'	7		27	40	ns
tPLH .		QA thru QH			17	25	
<sup>t</sup> PHL	CLK	QA IIII QH	$R_1 = 665 \Omega$ , $C_1 = 45 pF$		26	39	ns
<sup>t</sup> PHL	CLR	QA thru QH	11 000 32, 00 10 01		26	40	ns
<sup>t</sup> PZH	G1, G2	QA thru QH	7		13	21	
<sup>t</sup> PZL	01,02	α <sub>A</sub> tinα α <sub>H</sub>			19	30	ns
<sup>t</sup> PHZ	G1, G2	QA thru QH	R <sub>L</sub> = 665 Ω, C <sub>L</sub> = 5 pF		10	20	
<sup>t</sup> PLZ	] 31, 32	QA IIIIO QH			10	15	ns

 $<sup>\</sup>P_{\mathsf{fmax}} \equiv \mathsf{maximum} \; \mathsf{clock} \; \mathsf{frequency}$ 



 $<sup>^{\</sup>ddagger}$ All typical values are at  $V_{CC}$  = 5 V,  $T_{A}$  = 25°C.

<sup>§</sup>Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

tplH = propagation delay time, low-to-high-level output.

tpHL = propagation delay time, high-to-low-level output

 $t_{PZH} = output$  enable time to high level

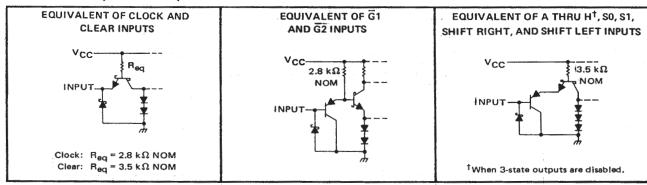
 $t_{PZL} \equiv output$  enable time to low level

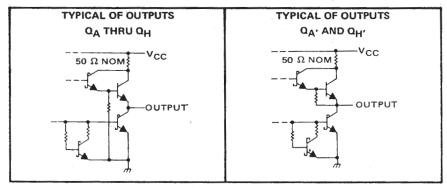
tpHZ ≡ output disable time from high level

 $t_{PLZ} \equiv output disable time from low level$ 

NOTE 2: For testing f<sub>max</sub>, all outputs are loaded simultaneously, each with C<sub>L</sub> and R<sub>L</sub> as specified for the propagation times, Load circuits and voltage waveforms are shown in Section 1.

#### schematics of inputs and outputs





### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC (see Note 1)
Input voltage
Off-state output voltage
Operating free-air temperature range: SN54S299 (See Note 1)55°C to 125°C
SN74S299 0 °C to 70 °C
Storage temperature range65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

#### recommended operating conditions

		SN54S299				N74S29	9	
		MIN	NOM	MAX	MIN	NOM	MAX	TINU
Supply voltage, V <sub>CC</sub>		4.5	5	5.5	4.75	5	5.25	V
High-level output current, IOH	QA thru QH			-2			-6.5	
riigii-iever output current, 10H	QA' or QH'			-0.5			-0.5	mA
Low-level output current, IOL	Q <sub>A</sub> thru Q <sub>H</sub>			20			20	mA
	QA' or QH'			6			6	I IIIA
Clock frequency, fclock		0		50	0		50	MHz
Width of clock pulse, tw(clock)	Clock high	10			10			
	Clock low	10			10			ns
Width of clear pulse, tw(clear)	Clear low	10			10			ns
	Select	15↑			15↑			
Setup time, t <sub>SU</sub>	High-level data <sup>‡</sup>	7↑			7↑			
Setup time, tsu	Low-level data <sup>‡</sup>	5↑			5↑			ns
	Clear inactive-state	10↑			10↑			
Hold time, th	Select	5↑			51			
Tiold time, th	Data <sup>‡</sup>	5↑			5↑			ns
Operating free-air temperature, TA		-55		125	0		70	°c

<sup>&</sup>lt;sup>‡</sup> Data includes the two serial inputs and the eight input/output data lines.



# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER		TEST CON	DITIONS	MIN	TYP‡	MAX	UNIT
VIH	High-level input voltage				2			V
VIL	Low-level input voltage						0.8	V
VIK	Input clamp voltage		V <sub>CC</sub> = MIN,	I <sub>I</sub> = -18 mA		-	-1.2	V
Vон	High-level output voltage	QA thru QH	VCC = MIN,	V <sub>IH</sub> = 2 V,	2.4	3.2		
* On		QA' or QH'	V <sub>IL</sub> = 0.8 V,		2.7	3.4		V
VOL	Low-level output voltage		V <sub>CC</sub> = MIN,	V <sub>IH</sub> = 2 V,				
- 01			V <sub>IL</sub> = 0.8 V,	IOL = MAX			0.5	٧
lozh	Off-state output current,	0 45 0	VCC = MAX,	V <sub>IH</sub> = 2 V,				
-0211	high-level voltage applied	Q <sub>A</sub> thru Q <sub>H</sub>	V <sub>O</sub> = 2.4 V				100	μА
IOZL	Off-state output current,	0 1 0		V <sub>IH</sub> ≈ 2 V,				
102L	low-level voltage applied	Q <sub>A</sub> thru Q <sub>H</sub>	V <sub>O</sub> = 0.5 V				-250	μА
11	Input current at maximum input voltage		V <sub>CC</sub> = MAX,	V <sub>I</sub> = 5.5 V			1	mA
чн	High-level input current	A thru H, S0, S1					100	IIIA
-111		Any other	V <sub>CC</sub> = MAX,	V <sub>1</sub> = 2.7 V			50	μА
		CLK or CLR					-2	mA
HL	Low-level input current	S0, S1	V <sub>CC</sub> = MAX,	V <sub>1</sub> = 0.5 V			-500	μΑ
		Any other		- '			-250	μА
los	Short-circuit output current§	Q <sub>A</sub> thru Q <sub>H</sub>			-40		-100	·····
-03	Short surface output contents	QA' or QH'	V <sub>CC</sub> = MAX	l	-20		-100	mA
lcc	Supply current		V <sub>CC</sub> = MAX			140	225	mA

 $<sup>^\</sup>dagger$  For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

# switching characteristics, $V_{CC} = 5 \text{ V}$ , $T_A = 25^{\circ} \text{ C}$

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	ТҮР	MAX	UNIT
f <sub>max</sub>			See Note 2	50	70		MHz
<sup>†</sup> PLH	CLK	Q <sub>A</sub> ' or Q <sub>H</sub> '	B. = 1 kg		12	20	
<sup>t</sup> PHL		da or dh	$R_L = 1 k\Omega$ , $C_L = 15 pF$		13	20	ns
<sup>†</sup> PHL	CLR	QA' or QH'			14	21	ns
<sup>t</sup> PLH	CLK	O			15	21	
<sup>t</sup> PHL		QA thru QH			15	21	ns
tPHL	CLR	QA thru QH	$R_L = 280 \Omega$ , $C_L = 45 pF$ .		16	24	ns
<sup>t</sup> PZH	Ğ1, Ğ2	0 11 0	1		10	18	
<sup>t</sup> PZL	01,02	QA thru QH			12	18	ns
<sup>t</sup> PHZ	G1, G2		$R_1 = 280 \Omega$ , $C_1 = 5 pF$		7	12	
<sup>t</sup> PLZ	G1, G2	• QA thru QH			7	12	ns

<sup>¶</sup>f<sub>max</sub> = maximum clock frequency

NOTE 2: For testing  $f_{\text{max}}$ , all outputs are loaded simultaneously, each with  $C_L$  and  $R_L$  as specified for the propagation times. Load circuits and voltage waveforms are shown in Section 1.



<sup>‡</sup>All typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25 ^{\circ} \text{C}$ .

<sup>§</sup> Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

tpLH = Propagation delay time, low-to-high-level output

tpHL = Propagation delay time, high-to-low-level output

tpzH = output enable time to high level

tpzL = output enable time to low level

tpHZ = output disable time from high level

tpLZ = output disable time from low level

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interface.ti.com	Digital Control	www.ti.com/digitalcontrol
logic.ti.com	Military	www.ti.com/military
power.ti.com	Optical Networking	www.ti.com/opticalnetwork
microcontroller.ti.com	Security	www.ti.com/security
www.ti.com/lpw	Telephony	www.ti.com/telephony
	Video & Imaging	www.ti.com/video
	Wireless	www.ti.com/wireless
	dataconverter.ti.com dsp.ti.com interface.ti.com logic.ti.com power.ti.com microcontroller.ti.com	amplifier.ti.com dataconverter.ti.com dsp.ti.com dsp.ti.com interface.ti.com logic.ti.com power.ti.com microcontroller.ti.com www.ti.com/lpw  Audio Audio Audio Audio Automotive Broadband Digital Control Military Optical Networking Security Telephony Video & Imaging

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DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
Low Power Wireless	www.ti.com/lpw	Telephony	www.ti.com/telephony
		Video & Imaging	www.ti.com/video
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Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
Low Power Wireless	www.ti.com/lpw	Telephony	www.ti.com/telephony
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Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
Low Power Wireless	www.ti.com/lpw	Telephony	www.ti.com/telephony
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Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
Low Power Wireless	www.ti.com/lpw	Telephony	www.ti.com/telephony
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Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
Low Power Wireless	www.ti.com/lpw	Telephony	www.ti.com/telephony
		Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless







## **PACKAGING INFORMATION**

Orderable Device	ce Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
78024012A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
7802401RA	ACTIVE	CDIP	J	20	1	TBD	A42 SNPB	N / A for Pkg Type
7802401RA	ACTIVE	CDIP	J	20	1	TBD	A42 SNPB	N / A for Pkg Type
7802401SA	ACTIVE	CFP	W	20	1	TBD	Call TI	N / A for Pkg Type
7802401SA	ACTIVE	CFP	W	20	1	TBD	Call TI	N / A for Pkg Type
SN54LS299J	ACTIVE	CDIP	J	20	1	TBD	A42 SNPB	N / A for Pkg Type
SN54LS299J	ACTIVE	CDIP	J	20	1	TBD	A42 SNPB	N / A for Pkg Type
SN54S299J	OBSOLETE	CDIP	J	20		TBD	Call TI	Call TI
SN54S299J	OBSOLETE	CDIP	J	20		TBD	Call TI	Call TI
SN74LS299DW	/ ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS299DW	/ ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS299DWE	4 ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS299DWE	4 ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS299DW0	64 ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS299DW0	64 ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS299DW	R ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS299DW	R ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS299DWR	E4 ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS299DWR	E4 ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS299DWR	G4 ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS299DWR	G4 ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS299N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LS299N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LS299NE	4 ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LS299NE	4 ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74S299DW	OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI
SN74S299DW	OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI
SN74S299DWF	R OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI
SN74S299DWF	R OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI
SN74S299N	OBSOLETE	PDIP	N	20		TBD	Call TI	Call TI
SN74S299N	OBSOLETE	PDIP	N	20		TBD	Call TI	Call TI





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Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp (3)
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SN74S299N3	OBSOLETE	PDIP	N	20		TBD	Call TI	Call TI
SNJ54LS299FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
SNJ54LS299FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
SNJ54LS299J	ACTIVE	CDIP	J	20	1	TBD	A42 SNPB	N / A for Pkg Type
SNJ54LS299J	ACTIVE	CDIP	J	20	1	TBD	A42 SNPB	N / A for Pkg Type
SNJ54LS299W	ACTIVE	CFP	W	20	1	TBD	Call TI	N / A for Pkg Type
SNJ54LS299W	ACTIVE	CFP	W	20	1	TBD	Call TI	N / A for Pkg Type
SNJ54S299FK	OBSOLETE	LCCC	FK	20		TBD	Call TI	Call TI
SNJ54S299FK	OBSOLETE	LCCC	FK	20		TBD	Call TI	Call TI
SNJ54S299J	OBSOLETE	CDIP	J	20		TBD	Call TI	Call TI
SNJ54S299J	OBSOLETE	CDIP	J	20		TBD	Call TI	Call TI
SNJ54S299W	OBSOLETE	CFP	W	20		TBD	Call TI	Call TI
SNJ54S299W	OBSOLETE	CFP	W	20		TBD	Call TI	Call TI

<sup>(1)</sup> The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <a href="http://www.ti.com/productcontent">http://www.ti.com/productcontent</a> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

**Pb-Free** (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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### TAPE AND REEL INFORMATION





Α	0	Dimension designed to accommodate the component width
В	0	Dimension designed to accommodate the component length
		Dimension designed to accommodate the component thickness
٧	٧	Overall width of the carrier tape
ГР	1	Pitch between successive cavity centers

## QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

Device		Package Drawing			Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LS299DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1





#### \*All dimensions are nominal

ĺ	Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
	SN74LS299DWR	SOIC	DW	20	2000	346.0	346.0	41.0

# 14 LEADS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

### FK (S-CQCC-N\*\*)

#### **28 TERMINAL SHOWN**

#### **LEADLESS CERAMIC CHIP CARRIER**



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. The terminals are gold plated.
- E. Falls within JEDEC MS-004



# W (R-GDFP-F20)

# CERAMIC DUAL FLATPACK



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within Mil-Std 1835 GDFP2-F20



# DW (R-PDSO-G20)

# PLASTIC SMALL-OUTLINE PACKAGE



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-013 variation AC.



# N (R-PDIP-T\*\*)

# PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.



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